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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,084	12/30/2003	Kwan-Yong Lim	00939H-087800US	1874

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EXAMINER	
DANG, TRUNG Q	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 02/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,084	LIM ET AL.	
	Examiner	Art Unit	
	Trung Dang	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-16* is/are allowed.

6)☒ Claim(s) *1-4 and 10-12* is/are rejected.

7)☒ Claim(s) *5-9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/01/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-3, 10-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Weimer et al. (US. 6,291,868).

With reference to Figs.1-2, the prior art teaches the claimed invention in that it discloses method for fabricating a transistor with a polymetal gate electrode structure, comprising the steps of:

forming a gate insulation layer **106** on a substrate **10** (col. 2, lines 56-67);

forming a patterned gate stack structure **112** on the gate insulation layer, wherein the patterned stack structure includes a polysilicon layer **104** as a bottom layer and a metal layer **100** as an upper layer (col. 3, lines 52-55);

forming a CVD oxide spacers **114A**, **114B** as oxidation barriers along a profile containing the patterned gate stack structure and on the gate insulation layer at a predetermined temperature that prevents oxidation of the metal layer (col. 5, lines 14-21); and

performing a gate re-oxidation process (col. 5, lines 29-35).

Note that the CVD oxide spacers **114A** and **114B** are functioning as oxidation barriers therefore oxidation of the metal layer **100** is prevented. Also, see col. 5, lines 46-58 and col. 6, lines 1-5 for the disclosure of the re-oxidation process which employs selective oxidation of silicon over the metal, i.e., silicon is oxidized while the metal is not. Furthermore, the CVD (chemical vapor deposition) process inherently involves temperature so that decomposition of precursor gas can take place.

As for claims 2 and 11, see col. 3, lines 14-23 for the materials of the diffusion barrier layer **102**.

3. Claims 1, 3, 4, and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. (US 6,800,907).

With reference to Figs.3A-3C, the prior art teaches the claimed invention in that it discloses method for fabricating a transistor with a polymetal gate electrode structure, comprising the steps of:

forming a gate insulation layer **42** on a substrate **41**;

forming a patterned gate stack structure on the gate insulation layer, wherein the patterned stack structure includes a polysilicon layer **43** as a bottom layer and a metal layer **44** as an upper layer (Fig. 3A and col. 6, lines 20-23);

forming a PETEOS (plasma enhanced chemical vapor deposition, wherein TEOS is a precursor gas) oxide capping layer **47** along a profile containing the patterned gate stack structure and on the gate insulation layer at a predetermined temperature that prevents oxidation of the metal layer (col. 6, lines 42-56); and

performing a gate re-oxidation process (Fig. 3C and related text).

Allowable Subject Matter

4. Claims 5-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter:

Claim 5 and its dependent claims are allowable over prior art of record for the limitation regarding the formation of the silicon-based capping layer through the use of ALD (atomic layer deposition) technique that prevents oxidation of the metal layer.

6. Claims 13-16 are allowed over prior art of record.

7. The following is an examiner's statement of reasons for allowance:

Independent claim 13 and its dependent claims are allowed because the prior art of record does not teach or suggest the claimed processing step regarding the formation of a silicon oxide layer by performing an ALD technique that prevents oxidation of the metal layer in a polymetal gate stack structure.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trung Dang whose telephone number is 571-272-1857. The examiner can normally be reached on Mon-Friday 9:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trung Dang
Primary Examiner
Art Unit 2823

2/02/05